مسائل مخصوص در مدارهای الکترونیکی(25266)

طراحی مدارهای مجتمع مبتنی برFPGA/ASIC

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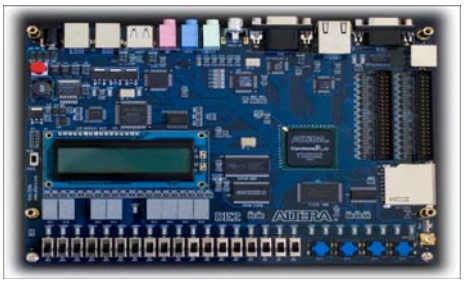

Altera DE2 board (used in this course)

Objective:

This course provides comprehensive theoretical understanding as well as exciting hands-on practical experience of the digital design flow, including the architecture optimization, hardware description languages (Verilog Coding), commercial Programmable Logic Designs (PLDs) and Field Programmable Gate Arrays (FPGAs) architectures, the physical realization steps in digital custom Application Specific Integrated Circuits (ASICs) design, as well as synthesis algorithms. Students will earn invaluable experience to professionally work with state-of-the-art design tools for both FPGA and ASIC design flow through several hardware implementation assignments. The implementation platform is Altera DE2 board (shown above), which will be used throughout the course. Moreover, students will design a ready-for-fabrication ASIC as a final project in this course. The brief syllabus of the course is as follows:

1. Hardware Description Language

- **Verilog Fundamentals**
  - Language Fundamentals
  - Modeling Combinational/Sequential Logic Circuits
  - Modeling Finite State Machines
- **Verilog for Verification**
  - Verification/Simulation techniques with test-benches
- **Verilog for synthesis**
  - Verilog Styles for Synthesis
  - Architectural techniques for high-speed designs (parallel proc., pipelining, retiming, …)
  - Implementations of common operations (complex multiplication, division, complex norm, CORDIC)
  - Fundamentals of fixed-point realization

2. PLDs & FPGA Architectures

- **FPGA Technologies**
  - SPLDs (PAL and PLA architectures)
  - Commercial CPLD Architectures
  - Anti-fuse Based FPGAs
  - Flash Based FPGAs
- **FPGA Technologies & Applications**
  - SRAM/LUT Based FPGAs
  - Anti-fuse/MUX Based FPGAs
  - Flash Based FPGAs

- **FPGA Architectures**
  - Heterogeneous/Homogeneous FPGAs
  - Fine-grained, coarse-grained and platform FPGAs
- **FPGA Elements & Design Trade-offs**
  - Logic Cells Common Architectures
  - Programmable Routing Channels Design
  - I/O & Pad architectures
- **Commercial FPGAs**
  - Altera (FLEX 10K, Stratix II,III) , Xilinx (XC4000, Virtex II,4,5), Actel (Act3, Axcelerator) FPGAs
- **FPGA Tools**
  - Altera Quartus
  - Xilinx ISE
  - Modelsim
  - TCL scripting

3. ASIC Design Flow

- **HDL Coding & Verification**
- **Synthesis & Timing Optimization**
  - Complete Synopsys Design Complier Design Flow
- **Physical Design**
  - Cadence First Encounter
  - Floorplan (Initial floorplan and power planning)
  - Placement (Full-scale floorplan and clock tree insertion)
  - Routing (power routing & Nanoroute)
  - Timing Closure (Analysis & Optimization of setup and hold time violations)
  - Fill (Filler Cells, Metal Fill, and Verify Geometry)

4. Synthesis Algorithms

- **Two-level Logic Optimization**
  - Quine-McClusky
- **Multi-level Logic Optimization**
  - BDDs
  - Boolean Satisfiability

Assignments:

There are several theoretical and practical assignments in the course. The ultimate goal is to educate and empower students to work as a professional FPGA/ASIC designer. Most of the assignments should be implemented and tested online on the DE2 board.

Final Project:

The final project is to implement a fairly large system on hardware. Students have the option to choose either the FPGA (DE2 board) or ASIC platform. The project is based on the current state-of-the art commercial IEEE standards. It is instructive for students to face the practical challenges as well as to become familiar with typical structure and design challenges of an IEEE standard. The suggested topics will be provided by the instructor while students are more than welcome to provide their proposals. Since DE2 board is a great platform for voice/video processing type of systems with enriched interfaces, several interesting projects can be defined.